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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/038,478	BRATT ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006 and 28 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-33 and 35-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-33 and 35-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-33, and 35-50 have been considered. Claims 4, 5, 20, 28, and 29 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 21 August 2006 and Amendment as received on 28 November 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11-24 and 35-48 are rejected under 35 U.S.C. 102(e) as being taught by Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari).

5. Referring to claims 11 and 35, taking claim 11 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. Receiving a first vector having a plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

c. Partitioning look-up memory into a plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

d. Looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

e. Wherein the partitioning and the looking-up operations are performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

6. Claim 35 is nearly identical to claim 11, differing in it's a method being comprised upon a machine-readable medium, but encompassing the same scope as claim 11. Therefore, claim 35 is rejected for the same reasons as claim 11.

7. Referring to claims 12 and 36, taking claim 12 as exemplary, Sazegari has taught a method as in claim 11 wherein the receiving the first vector having a plurality of numbers comprises partitioning a string of bits into a plurality of segments to generate the plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-

63; Figure 2, Figure 4; and Figure 6).

8. Referring to claims 13 and 37, taking claim 13 as exemplary, Sazegari has taught a method as in claim 12 wherein the single instruction specifies format information in which the plurality of numbers are stored in the string of bits (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

9. Referring to claims 14 and 38, taking claim 14 as exemplary, Sazegari has taught a method as in claim 11

a. Wherein the look-up memory comprises a plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6), and

b. Wherein said partitioning look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

10. Referring to claims 15 and 39, taking claim 15 as exemplary, Sazegari has taught a method as in claim 12 wherein the string of bits is received from an entry of a register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

11. Referring to claims 16 and 40, taking claim 16 as exemplary, Sazegari has taught a method as in claim 15 wherein the single instruction specifies an index of the entry (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

12. Referring to claims 17 and 41, taking claim 17 as exemplary, Sazegari has taught a method as in claim 11 further comprising storing the second vector having the plurality of elements in an entry of a register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

13. Referring to claims 18 and 42, taking claim 18 as exemplary, Sazegari has taught a method as in claim 17 wherein the single instruction species an index of the entry (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

14. Referring to claims 19 and 43, taking claim 19 as exemplary, Sazegari has taught a method as in claim 17 wherein the single instruction specifies format information in which the plurality of elements are stored in the entry (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

15. Referring to claims 20 and 44, taking claim 20 as exemplary, Sazegari has taught a method as in clam 11 the look-up memory comprises a plurality of look-up units, and

a. Wherein said partitioning look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

b. Wherein each of the plurality of look-up units comprises 256 8-bit entries (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

16. Referring to claims 21 and 45, taking claim 21 as exemplary, Sazegari has taught a

method as in claim 11 wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

17. Referring to claims 22 and 46, taking claim 22 as exemplary, Sazegari has taught a method as in claim 21 wherein the total number of entries is one of:

a. 256 (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. 512; and

c. 1024.

18. Referring to claims 23 and 47, taking claim 23 as exemplary, Sazegari has taught a method as in claim 11 wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

19. Referring to claims 23 and 48, taking claim 24 as exemplary, Sazegari has taught a method as in claim 21 wherein the total number of bits is one of:

a. 8 (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. 16; and

c. 24.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 1-9, 25-33, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari) in view of Barry et al., U.S. Patent Number 6,397,324 (herein referred to as Barry) and in further view of Priem, U.S. Patent Number 5,768,628 (herein referred to as Priem).

22. Referring to claims 1 and 25, taking claim 1 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. Receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

c. Operating on simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

d. Wherein the receiving and the operating operations are performed in response to

the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

23. Sazegari has not taught the operation being replacing. Barry has taught replacing data simultaneously in the look-up tables (Barry Col.9 lines 41-62 and Col.12 lines 14-27). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized the simultaneous storing of data in a look-up table increases efficiency for processing compressed data (Barry column 1, lines 66-67 and column 2, lines 40-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the store operation of Barry in the device of Sazegari to improve compressed data processing efficiency.

24. In addition, Sazegari has not taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit. Priem has taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

25. Claim 25 is nearly identical to claim 1, differing in its method being comprised upon a machine-readable medium, but encompassing the same scope as claim 1. Therefore, claim 25 is rejected for the same reasons as claim 1.

26. Referring to claims 2 and 26, taking claim 2 as exemplary, Sazegari has taught a method as in claim 1, wherein the first vector having the first plurality of numbers are is received from a first entry in a register file; and the second vector having the second plurality of numbers are is received from a second entry in the register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

27. Referring to claims 3 and 27, taking claim 3 as exemplary, Sazegari has taught a method as in claim 2 wherein the single instruction specifies indices of the first and second entries in the register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

28. Referring to claims 4 and 28, taking claim 4 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction having a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

b. Operating on at least one entry in at least one of a plurality of look-up units in a microprocessor unit with at least one number (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and

Figure 6);

c. Wherein the operating is performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

29. Sazegari has not taught the operation being replacing. Barry has taught replacing data simultaneously in the look-up tables (Barry Col.9 lines 41-62 and Col.12 lines 14-27). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized the simultaneous storing of data in a look-up table increases efficiency for processing compressed data (Barry column 1, lines 66-67 and column 2, lines 40-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the store operation of Barry in the device of Sazegari to improve compressed data processing efficiency.

30. Sazegari has not taught using

a. The instruction having an identity number code that specifies a DMA controller; and

b. Using the Direct Memory Access (DMA) controller.

31. Priem has taught using

a. The instruction having an identity number code that specifies a DMA controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4); and

b. Using the Direct Memory Access (DMA) controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and

Figure 4).

32. In regards to Priem, the wave tables are transferred vie the sound card's sound generation controller's DMA in response to CPU commands, e.g. instructions, that identify the sound tables need to be loaded. In other words, the CPU commands to transfer the sound tables identify and command the sound controller, and in turn the DMA controller, to transfer the tables. A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

33. Claim 28 is nearly identical to claim 4, differing in its method being comprised upon a machine-readable medium, but encompassing the same scope as claim 4. Therefore, claim 28 is rejected for the same reasons as claim 4.

34. Referring to claims 5 and 29, taking claim 5 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction having a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

b. Operating on at least one entry for each of a plurality of look-up units in a

microprocessor with a plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

c. Wherein the operating is performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

35. Sazegari has not taught the operation being replacing. Barry has taught replacing data simultaneously in the look-up tables (Barry Col.9 lines 41-62 and Col.12 lines 14-27). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized the simultaneous storing of data in a look-up table increases efficiency for processing compressed data (Barry column 1, lines 66-67 and column 2, lines 40-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the store operation of Barry in the device of Sazegari to improve compressed data processing efficiency.

36. Sazegari has not taught using

a. The instruction having an identity number code that specifies a DMA controller; and

b. Using the Direct Memory Access (DMA) controller.

37. Priem has taught using

a. The instruction having an identity number code that specifies a DMA controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4); and

b. Using the Direct Memory Access (DMA) controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4).

38. In regards to Priem, the wave tables are transferred vie the sound card's sound generation controller's DMA in response to CPU commands, e.g. instructions, that identify the sound tables need to be loaded. In other words, the CPU commands to transfer the sound tables identify and command the sound controller, and in turn the DMA controller, to transfer the tables. A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

39. Claim 29 is nearly identical to claim 5, differing in its method being comprised upon a machine-readable medium, but encompassing the same scope as claim 5. Therefore, claim 29 is rejected for the same reasons as claim 5.

40. Referring to claims 6 and 30, taking claim 6 as exemplary, Sazegari has taught a method as in claim 5 wherein a single index encoded in the instruction specifies a location of the at least one entry in the plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

41. Referring to claims 7 and 31, taking claim 7 as exemplary, Sazegari has taught a method as in claim 5 wherein a single index encoded in the instruction specifies a total number of the at

least one entry for each of a plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

42. Referring to claims 8 and 32, taking claim 8 as exemplary, Sazegari has taught a method as in claim 5 wherein a source address of the plurality of numbers in host memory is specified in an entry of a register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

43. Referring to claims 9 and 33, taking claim 9 as exemplary, Sazegari has taught a method as in claim 8 wherein the single instruction specifies an index of the entry in the register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

44. Referring to claim 49, Sazegari has taught a method as in claim 5 wherein the at least one entry for each of the plurality of look-up units comprises a plurality of entries for each of the plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

45. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari), as applied to claim 11 above, and in further view of Priem, U.S. Patent Number 5,768,628 (herein referred to as Priem). Sazegari has not taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit. Priem has taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the

art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

Response to Arguments

46. Examiner withdraws claim objections to claims 20 and 28 in favor of the amended claims.

47. Applicant argues in essence on pages 12-14

> Thus, Sazegari merely discloses simultaneously reading values of two vectors from a single table according to index values stored in the register. In contrast...refers to looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers of a first vector.

48. This has not been found persuasive. The limitation argued explicitly states in the claim "looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up table and being pointed to by one of the plurality of number..." Applicant's arguments characterize Sazegari's invention as "simultaneously reading values of two vectors from a single table according to index values stored in the register." This is a very broad sweeping characterization

that is not entirely correct. As background, Sazegari explains with reference to Figures 3 and 4 and in column 4, lines 5-46, a permute instruction "operates to fill a register with data values from two other registers (Sazegari column 4, lines 7-9)." However, as Sazegari states in column 1, lines 51-55, for tables with more than two registers of data, "it is no possible to utilize the permute operation for[*sic*] perform vector execution". Therefore, the system loses benefits, such as significantly increasing processing speed by performing simultaneous table look-ups, of vector-based processing. As Sazegari states in column 2, lines 17-20 "In accordance with the invention, this objective is achieved by logically dividing a large table into a number of smaller tables that can be uniquely indexed with a permute instructions." The larger table referred to in Sazegari is similar to claim 11's language for a "look-up memory", and, since Sazegari divides the larger look-up table into smaller tables, the limitation "partitioning look-up memory into a plurality of look-up tables" is met. Sazegari shows by example in Figures 6, 7a-7c, and 8a-8h and explains in column 6, lines 1-44, a large look-up memory, e.g. 64-byte entry table, is separated, e.g. partitioned, into smaller look-up tables, e.g. two of the four 16-byte data vectors. As Sazegari explains in column 4, lines 23-46 with reference to Figure 3, a permute instruction is used to simultaneously select multiple elements from the look-up table to find an intermediate result. However, since there are now multiple look-up tables, the same permutation instruction is performed multiple times: once on each of the smaller look-up tables. The remaining bits of the original instruction are then used to select data from the intermediate result vectors to find a final result. Sazegari's specific examples in Figures 6 and 10 have either a larger table, e.g. look-up memory, of 64-byte entries or 128-byte entries. Sazegari divides the larger tables into two and four smaller look-up tables respectively, so a permute instruction can be used to access the

smaller tables to find the intermediate vector results V_{12}, V_{34}, V_{56}, and V_{78}. The remaining bits of a permute instruction are used to select elements from the intermediate vector results to form a final vector result. Hence, the permute instruction produces intermediate result vectors containing values read simultaneously from the multiple smaller look-up tables specified by a mask, e.g. a first vector. Then the permute instruction provides selection information that selects values from intermediate result vectors to form a final vector result, e.g. second vector.

49. Applicant argues in essence on pages 14-15

> It is respectfully submitted that Sazegari does not teach or suggest a combination with Barry and Priem, Barry does not teach or suggest a combination with Sazegari and Priem, and Priem does not teach or suggest a combination with Sazegari and Barry...It would be impermissible hindsight, based on Applicants own disclosure, to combine Sazegari, Barry, and Priem.

50. This has not been found persuasive. Applicant's arguments appear to be focusing on the specific implementations of Sazegari, Barry, and Priem. However, the Examiner would like to point out that Sazegari, Barry, and Priem all involve accessing and using data stored in tables. In general, Sazegari is a method to access larger tables using vectors. Barry is about instructions for loading and storing information in tables. Priem is for accessing tables in system memory via a DMA for rapid transfer. To argue that Sazegari, Barry, and Priem are for different fields of endeavor is taking an extremely narrow interpretation of the references and field of art. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching,

suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation to combine Barry and Priem, which was stated by the Examiner in the previous rejection and has been copied above, were from explicit statements within Barry and Priem. The citations from Barry and Priem to support the Examiner's motivation were cited in the previous rejection, which has been copied above. Barry teaches in that digital signal processors need to provide the ability to efficiently process compressed data (Barry column 1, lines 66-67 and column 2, lines 40-42) and ability is at least partially achieved when incorporating his instructions. Priem teaches that process speed and efficiency is increased (Priem column 2, line 64 to column 3, line 5) when incorporating a dynamic memory controller to rapidly transfer data in the tables from system memory.

51. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

52. Applicant argues in essence on page 15

> ...such a combination would lack the following limitations of amended claim 4: receiving the single instruction having an identity number code that specifies a

DMA controller and a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up units.

53. This has not been found persuasive. As explained in the previous rejection, which as been copied above, the DMA controller responds to commands from the sound generation controller, which responds to commands from the CPU. The CPU generates its commands based upon the instructions executing, so, in order for the DMA controller to be utilized, an instruction must specify it for the CPU to generate the commands for the sound controller to utilize the DMA controller. The amended claim language now requires "a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up units" to be present in the references. Barry teaches this element, as shown in the rejection above. Barry shows in Figures 7a and 8a column 11, lines 49-63, bits 9 and 10 designate the number of table look-ups, specifically the table in lines 55-63 shows the specific number associated with the four possible bit combinations. Barry shows in Figure 7a a store to single table instruction with bits 9 and 10 being 01 respectively. In Figure 8a, a store to two tables instruction with bits 9 and 10 being 11. Barry describes with respect to the load two tables instruction that, which is also applicable to the store to two tables instruction, it is possible that identical tables are accessed based upon the base address and designation that the instruction is a two table instruction (Barry column 11, lines 4-13). When the base addresses are different or bits 9 and 10 indicate a single table look-up, then only one entry is loaded per designated table. Similarly, the number of entries accessed in a four table look-up is reflected in the base addresses bits and bits 9 and 10. Hence, Barry has taught the base address bits and bits 9 and 10, e.g. bit segment, indicates the number of entries loaded per table.

Conclusion

54. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

55. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

56. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

57. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

58. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li
16 February 2007

EDDIE CHAN
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